WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a memory;

a plurality of logic portions that are connectable to the memory and respectively carry out data processing; and

a separation portion that connects at least one of the plurality of logic portions to the memory while separating the other logic portion(s) from the memory.

2. The semiconductor integrated circuit according to claim 1, wherein

the plurality of logic portions have different functions; and

the separation portion connects a logic portion that has a function required by the semiconductor integrated circuit to the memory.

3. The semiconductor integrated circuit according to claim 1, wherein

the plurality of logic portions have the same function; and

of the plurality of logic portions, the separation portion connects to the memory a logic portion that has integrity.

4. The semiconductor integrated circuit according to claim 1, wherein

the separation portion comprises a plurality of fuse circuits arranged between the memory and the respective plurality of logic portions; and

a fuse of the fuse circuits that corresponds to the other logic portion(s) is severed.

5. The semiconductor integrated circuit according to claim 4, wherein

the severance of the fuse of the fuse circuits is accomplished in a process

of redundancy-based recovery of memory in a manufacturing process of the semiconductor integrated circuit.

6. The semiconductor integrated circuit according to claim 1, wherein

the separation portion comprises a plurality of antifuse circuits arranged between the memory and the respective plurality of logic portions; and

an antifuse of the antifuse circuits that corresponds to one of the logic portions is in a conductive state, while another antifuse of the antifuse circuits that corresponds to the other logic portion(s) is in a non-conductive state.

7. The semiconductor integrated circuit according to claim 1, wherein

the separation portion comprises switching circuits arranged between the memory and the plurality of logic portions; and

each of the switching circuits, in regard to each logic portion, performs switching control in response to a received control signal, switching between a connected state, in which the corresponding logic portion and the memory are connected, and a separated state, in which the corresponding logic portion and the memory are separated.

8. The semiconductor integrated circuit according to claim 7, wherein

the switching circuits are arranged between the memory and the respective plurality of logic portions, and comprise a plurality of transistor switches that, in response to the control signals, perform respective open/close operations; and

each of the transistor switches realizes the connected state by closing, while realizing the separated state by opening.

9. The semiconductor integrated circuit according to claim 7, further

comprising:

a control signal fixing circuit that fixes the control signal into either the connected state or the separated state.

10. The semiconductor integrated circuit according to claim 7, wherein at least one of the plurality of logic portions comprises:

a control circuit that judges whether or not said at least one logic portion is accessing the memory, and, based on the result of this judgment, outputs the control signal such that said at least one logic portion goes into either the connected state or the separated state.

11. The semiconductor integrated circuit according to claim 10, wherein

the control circuit, when said at least one logic portion is not required by the semiconductor integrated circuit, outputs the control signal such that said at least one logic portion goes into the separated state.

12. The semiconductor integrated circuit according to claim 7, wherein at least one of the plurality of logic portions comprises:

a control circuit that, when judging that a logic portion other than said at least one logic portion is in an inoperative state, outputs the control signal such that the logic portion other than said at least one logic portion goes into the separated state.

13. The semiconductor integrated circuit according to claim 7, wherein

the memory comprises a request signal generating circuit that outputs a request signal to at least one of the plurality of logic portions; and

said at least one logic portion comprises:

a control circuit that judges an operative state of said at least one logic portion when the request signal is received and, based on the result of this judgment, outputs the control signal such that said at least one logic portion goes into either the connected state or the separated state.

14. The semiconductor integrated circuit according to claim 7, further comprising:

a test circuit that determines the integrity of each logic portion and outputs a determination signal based on the result of this determination to said each logic portion;

wherein at least one of the plurality of logic portions is provided with:

a control circuit that receives the determination signal, and, when the determination signal indicates that said at least one logic portion lacks integrity, outputs the control signal such that said at least one logic portion goes into the separated state.

15. The semiconductor integrated circuit according to claim 7, further comprising:

a test circuit that determines the integrity of each logic portion and outputs the control signal such that a logic portion determined to be lacking integrity goes into the separated state.

16. The semiconductor integrated circuit according to claim 1, further comprising:

a power source separation circuit that separates the logic portion that is in a separated state from the power source supplied to that logic portion.

17. The semiconductor integrated circuit according to claim 1, further comprising:

a substrate voltage changing circuit that, in order to lessen the difference between a power source voltage supplied to a logic portion in the separated state and the substrate voltage of the corresponding logic portion, changes the corresponding substrate voltage.

18. The semiconductor integrated circuit according to claim 1, wherein

the separation portion selectively connects, of the plurality of logic portions, a used logic portion, which is used by the semiconductor integrated circuit, to the memory, while separating from the memory an unused logic portion, which is a logic portion other than the used logic portion.

19. The semiconductor integrated circuit according to claim 18, wherein

the logic portions can be selectively connected to an output circuit inside the memory; and

the separation portion is arranged between the output circuit and the logic portions, connecting the used logic portion to the output circuit, while separating the unused logic portion from the output circuit.

20. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of output circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to an amp circuit inside the memory via the respective corresponding ones of the output circuits; and

the separation portion is arranged between the amp circuit and the output circuits, connecting the used logic portion to the amp circuit, while separating the

unused logic portion from the amp circuit.

21. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of output circuits and a plurality of amp circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to a preamp circuit inside the memory via the respective corresponding ones of the output circuits and amp circuits; and

the separation portion is arranged between the preamp circuit and the amp circuits, connecting the used logic portion to the preamp circuit, while separating the unused logic portion from the preamp circuit.

22. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of output circuits, a plurality of amp circuits, and a plurality of preamp circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to a sense amp circuit inside the memory via the respective corresponding ones of the output circuits, amp circuits, and preamp circuits; and

the separation portion is arranged between the sense amp circuit and the preamp circuits, connecting the used logic portion to the sense amp circuit, while separating the unused logic portion from the sense amp circuit.

23. The semiconductor integrated circuit according to claim 18, wherein

the logic portions can be selectively connected to an input circuit inside the memory; and

the separation portion is arranged between the input circuit and the logic

portions, connecting the used logic portion to the input circuit, while separating the unused logic portion from the input circuit.

24. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of input circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to a write amp circuit inside the memory via the respective corresponding ones of the input circuits; and

the separation portion is arranged between the write amp circuit and the input circuits, connecting the used logic portion to the write amp circuit, while separating the unused logic portion from the write amp circuit.

25. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of input circuits and a plurality of write amp circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to a write buffer circuit inside the memory via the respective corresponding ones of the input circuits and write amp circuits; and

the separation portion is arranged between the write buffer circuit and the write amp circuits, connecting the used logic portion to the write buffer circuit, while separating the unused logic portion from the write buffer circuit.

26. The semiconductor integrated circuit according to claim 18, wherein

the memory has a plurality of input circuits, a plurality of write amp circuits, and a plurality of write buffer circuits respectively corresponding to the plurality of logic portions;

the logic portions can be selectively connected to a sense amp circuit inside

the memory via the respective corresponding ones of the input circuits, write amp circuits, and write buffer circuits; and

the separation portion is arranged between the sense amp circuit and the write buffer circuits, connecting the used logic portion to the sense amp circuit, while separating the unused logic portion from the sense amp circuit.